What is claimed is:

1. A data transmission system for the serial asynchronous data transmission between a first unit (1) and a second unit (3),

- each of the units (1; 3) being assigned a circuit part (2; 4);
- and each of the circuit parts (2; 4) featuring a receiver circuit part (2b; 4b) and a transmitter circuit part (2a; 4a) having a transmitter terminal (Tx_Ew; Tx_CPU) and a receiver terminal (Rx_Ew; Rx_CPU) as well as a terminal for a data transmission line (8b) and a terminal for a reference potential line (8a).
- and the circuit parts (2; 4) being interconnectable via the data transmission line (8b) for bidirectional data transmission and via the reference potential line (8a),

wherein a current source (6) exists via which a current (Iq) can be fed into the data transmission line (8a) in such a manner that, depending on the signal state of a transmitter terminal (Tx_Ew; Tx_CPU) of the respective circuit part (4; 2), the signal state of the each case assigned receiver terminal (Rx_CPU; Rx_Ew) of the other circuit part (2; 4) can be changed.

2. The data transmission system as recited in Claim 1;

wherein at least the first unit (1) is a programmable small control system having a processing unit, in particular a microcontroller, a display unit, an operating control unit, signal inputs and signal outputs,

the processing unit, the display screen, the operating control unit, the signal inputs and the signal outputs being accommodated in a common housing.

3. The data transmission system as recited in Claim 1;

wherein at least the first unit (1) is designed as a separate module for connection to a programmable small control system having a processing unit, in particular a microcontroller, a display unit, an operating control unit, signal inputs and signal outputs,

the processing unit, the display screen, the operating control unit, the signal inputs and

the signal outputs being accommodated in a common housing.
and the second unit (3) being as designed as a separate module for the connection of a device which expands the functions of the first unit (1),
and both modules being connectable via the data transmission line (8b) and the reference potential line (8a).

4. The data transmission system as recited in Claims 1 through 3;
wherein the current source (6) is integrated in the second unit (3).

5. The data transmission system as recited in Claims 1 through 4;
wherein each receiver- and transmitter circuit part (2b, 4b; 2a, 4a) contains at least one semiconductor switch.

6. The data transmission system as recited in Claims 1 through 5;
wherein the receiver- and transmitter circuit parts (2b, 2a) of the first unit (1) are designed in such a manner that a galvanic separation is guaranteed, on one hand, between the transmitter terminal and the receiver terminal (Tx_CPU, Rx_CPU) and, on the other hand, between the terminals for the data transmission line and the reference potential line.

7. The data transmission system as recited in Claims 1 through 6;
wherein the current source (6) is designed as a constant current source.

8. The data transmission system as recited in Claim 7;
wherein the current source (6) is formed by a p-n-p transistor (T2) which is connected to a supply potential via an ohmic resistor (R2) on the emitter side,
the transistor (T2) being also connected to the supply potential via a Zener diode D2 on the base side as well as to the reference potential via a further ohmic resistor and, via its collector terminal, to the data transmission line (8b ).

9. The data transmission system as recited in one of the Claims 1 through 6;

wherein the current source (6) is constituted by an ohmic resistor which is connected to the supply potential via its one end and to the data transmission line (8b) via its other end.